

Appl. No. : 09/853,998
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IN THE SPECIFICATION:

Please amend the specification as follows:

(1) The paragraph from page 4, line 30 to page 5, line 6 has been amended as follows:

The ~~inverse~~ inversion request signal 110s is to produce write data such as "1" for a specified memory cell when the write data for all other neighboring memory cells is "0", or vice versa. Typically, a location of such a specified memory cell is shifted in a diagonal direction such as shown by hatched portions of Figure 4 to effectively detect "pattern sensitive faults". For performing such a test, the pattern generator PG generates the address data which increments by one to sequentially access the memory cells, and write data such as "0" for all of the memory cells, and an inversion request signal for a specified memory cell to invert the write data to "1".

(2) The paragraph from page 5, line 29 to page 6, line 6 has been amended as follows:

The X AND gate 32 is provided with the maximum X address value at one input while X address data is provided at another input. The Y AND gate 34 is provided with the maximum Y address value at one input while the added result YA from the accumulator 20 is provided at another input. The maximum X address value and maximum Y address value are provided as mask data for limiting an effective bit width in the 16-bit width

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of the address data based on the size of the DUT. For example, in the memory configuration shown in Figure 3, because the effective bit width is 2-bit, the mask data (maximum address value) expressed in a binary form is "0000,0000,0000,0011", thereby masking data bits higher than the first two bits.

(3) The paragraph from page 11, line 10 to page 11, line 17 has been amended as follows:

Twelfth, when the address of a memory cell is (X, Y) = (3, 2), the conditional equation of left side "(Y address of memory cell + diagonal inversion set value) AND maximum Y address value" is ~~(2 + 3) & 3 = 1~~ (2 + 3) AND 3 = 1, and the conditional equation of right side "(X address of memory cell AND maximum X address value)" is ~~3 & 3 = 3~~ 3 AND 3 = 3, thus, left side \neq right side. Therefore, the data is not inverted for the memory cell.

(4) The paragraph from page 18, line 26 to page 18, line 31 has been amended as follows:

It is, therefore, an object of the present invention to provide a pattern generator for a semiconductor test system which is capable of correctly generating an inversion request signal even if the memory device under test has different total numbers of memory cells between row (X) and column (Y) directions.

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(5) The paragraph from page 19, line 6 to page 19, line 16 has been amended as follows:

In order to solve the above problems, in the present invention, a pattern generator in a semiconductor test system for generating test patterns for testing a semiconductor memory device includes an inversion request signal circuit for generating an inversion request signal for each specified memory cell of the DUT for inverting write data to the specified memory cell in such a way that locations of specified memory cells are on a diagonal line on an array of memory cells in the semiconductor memory device wherein the numbers of overall memory cells in row (X) and column (Y) are different from each other.

(6) The paragraph from page 20, line 28 to page 21, line 2 has been amended as follows:

According to the present invention, the pattern generator for semiconductor test system is capable of correctly generating an inversion request signal even if the memory device under test has different total numbers of memory cells between X and Y directions. The pattern generator is able to invert the write data for memory cells on a specified diagonal line of the memory device without using a specific test program. Therefore, the present invention can improve test performance of memory devices with high test throughput and low cost.

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(7) The paragraph from page 22, line 14 to page 22, line 22 has been amended as follows:

Referring now to Figure 7, there is shown an inversion request signal circuit in a pattern generator in accordance with the present invention. The effect of the present invention using the circuit diagram of Figure 7 is shown in the schematic diagram of Figure 8. As shown in Figures 7 and 8, write data for specified memory cells in a diagonal line is correctly inverted when the memory device has different numbers of total memory cells between the X (row) and Y (column) directions.

(8) The paragraph from page 33, line 21 to page 33, line 30 has been amended as follows:

As has been described above, according to the present invention, the pattern generator for semiconductor test system is capable of correctly generating an inversion request signal even if the memory device under test has different numbers of total memory cells between X and Y directions. The pattern generator is able to invert the write data for memory cells on a specified diagonal line of the memory device without using a specific test program. Therefore, the present invention can improve test performance of memory devices with high test throughput and low cost.